

# Verification of Arbiter and Master of Advanced High Performance Bus using PSL

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**Abstract**— using assertion in any design plays a central role in the verification of the design and hence the demands of assertion based verification (ABV) grow rapidly in the verification field. PSL (property specification language) is assertion language used to verify the design. In this paper, the assertion based verification (ABV) of master and slaves of advanced high performance (AHB) bus of advanced microcontroller bus architecture (AMBA) is done by using PSL. The assertions are written in PSL language and verified in ModelSim. First an advanced high performance bus of three masters and four slaves is designed using verilog and assertions for the bus are implemented in PSL language and then verified it.

**Keywords** —Verification, PSL, AMBA-AHB, assertion.

## I. INTRODUCTION

Day by day verification of any design becomes a challenging task for the engineer as the complexity of the design grows rapidly with more number of functionality introduces in the same device with a critical situation that verification time increase up to 70-80% of the design time. More time are requires to verify the same device as device reusability increases. Verification of such complex designs has been left to simulation which has a drawback that verification with simulation is a very time consuming and lengthy process. So to minimize the time and to save money designer need a good verification methodology. ABV has recently gained popularity among verification engineer. Assertions represent desirable properties that a designer should satisfy. ABV is such a technique which combines simulation, assertion and formal technique to the traditional functional verification. Assertion is check embedded into the design to verify a designer's assumption about how a design should operate. One key characteristic of assertion is that it captures the correct design behavior one cycle by cycle basis and can accordingly be used to verify immediate behavior. As a result assertion can detect incorrect design properties at the time and place it happens. This improves to find the bugs without simulation

run in the design part only. ABV helps designer to finds the bug in the earlier stage of the design without caring the bugs in the later stage of the design because bugs which are not uncovered during earlier stage will carry on into later design stage, and fixing such bugs is a very expensive and time consuming process. ABV simplifies the diagnosis and detection of bugs by localizing the occurrence of a suspected bug to an assertion window, the assertion bug is then checked. It also increases both controllability and observability of a design. A good number of system design houses (e.g. IBM, Intel, more) employ this pre-RTL methodology, where a high-level description of the system is modelled in an FSM form and verified against the architectural requirements [4]. A different application to PSL is its extension to analog and mixed signal domain [5].

Standard assertion language used by the verification engineer is SystemVerilog Assertions (SVA) and Property Specification Language (PSL) from accellera to capture the functional specification of the design. The assertions for SystemVerilog assertion use systemverilog language where as the assertions for PSL can be written in Verilog, VHDL, System Verilog and SystemC flavor. Another assertion based verification technique by using Open Verification Library (OVL) is a library of predefined checkers written in Verilog or VHDL. Property Specification Language (PSL) is a multi-purpose, multi-level and multi-flavour assertion language. In the other hand SVA is tightly connected to the SystemVerilog language. In contrast Open Verification Library (OVL) is composed of asset of assertion checkers that verify only specific properties of a design with limited number of instruction set.

SystemVerilog Assertion adds features to specify assertion of a system. In SVA assertions can be used to provide functional coverage where as PSL is a separate languages specifically designed to work with many high levels languages. PSL provides the capability to write assertions that ranges from system level to RTL level. PSL has a rich set of

operators that can be used at different level of verification. The code used for PSL assertion is very less compared to SVA assertions. PSL can be placed directly in VHDL code but SVA cannot. PSL is a part of latest VHDL standard. PSL is devolved to provide means of specifying design properties. In verification stage, PSL is used to verify if a design satisfies all desired properties and specification. A PSL specification consists of assertions on different properties of a design

The paper discusses the verification of a widely used bus Advanced High Performance (AHB) bus of Advanced Microcontroller Bus Architecture (AMBA). The AMBA AHB bus architecture consists of three master and four slaves used for data transfer between the masters and the slaves. This paper organized as section (II) describes the designing of AMBA AHB and its architecture (III) describes the designing of AHB arbiter and master, in section (IV) the verification of AHB arbiter and master is analyzed and the section (v) discuss about the conclusion and future work.

II. DESIGNING OF AMBA AHB

The registered trademark of ARM Ltd is AMBA. The first AMBA buses were advanced system bus (ASB) and advanced peripheral bus (APB). In its second generation, AMBA 2, ARM added AMBA high performance bus (AHB) that is a single clock edge protocol. AMBA is an on-chip bus protocol from ARM. It is an open system on chip bus protocol for high performance buses on low power devices. AMBA has its vast number of buses in it. Of them Advanced high performance bus (AHB) is one of the most useful bus in any embedded system.

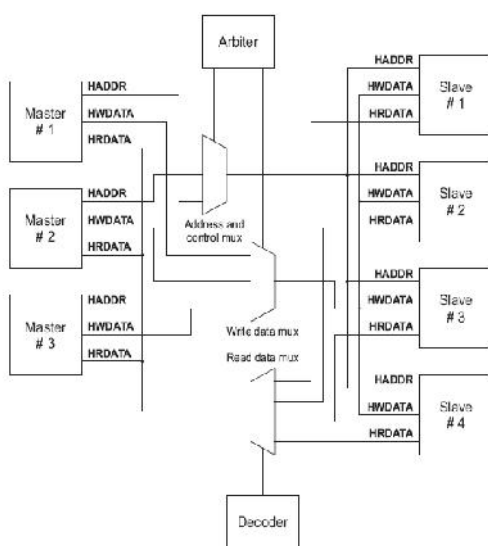


Figure 1: Architecture of the AMBA AHB

Figure 1 shows the architecture of AMBA AHB using 3 masters and 4 slaves. As shown in the figure the AMBA AHB

architecture has four components. The AMBA AHB can support up to 16 bus master. Each master wishing to initiate a transfer competes for a bus grant from the arbiter and has its control and address signal driven to the slave when it gets the bus. Bus master initiates read and write operations by providing address and control information. Only one bus master is allowed to use the bus actively. The arbiter is the main controlling element of the AHB bus. AHB arbiter ensures that only one bus master at a time is allowed to initiate data transfer and also gives priority to the master if more than one master is requested for the data transfer at a time. An AHB slaves respond to the read and write operation of the master. The AHB decoder is centralized decoder used to decodes the address to the selected slaves.

In our project we designed a advanced high performance bus using 3 masters and 4 slaves. We use verilog language for the designing of AHB bus. Figure 2 below shows the simulation result of the AMBA AHB.

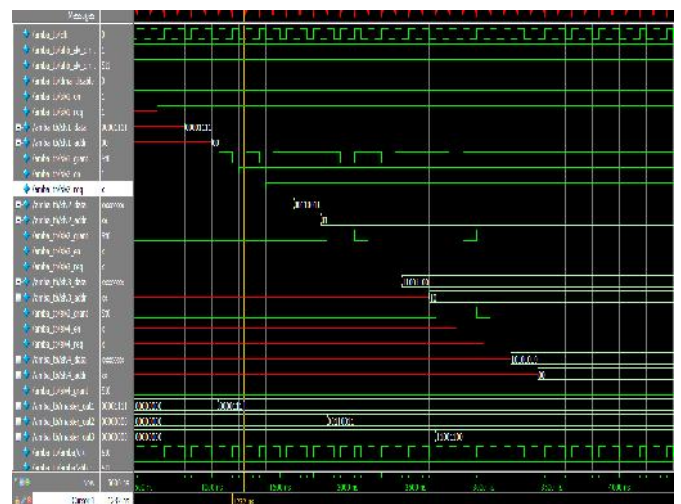


Figure: 2 Simulation result of the AMBA AHB

III. DESIGNING OF AHB ARBITER AND MASTER

AMBA AHB arbiter uses any of the arbitration algorithm or priority scheduling algorithm. In this research work we use round robin algorithm for the designing of the AHB arbiter. A round robin algorithm guarantees fairness among master and allowed unused time slot to be allocated to a master whose round robin turn is later but who is ready now.

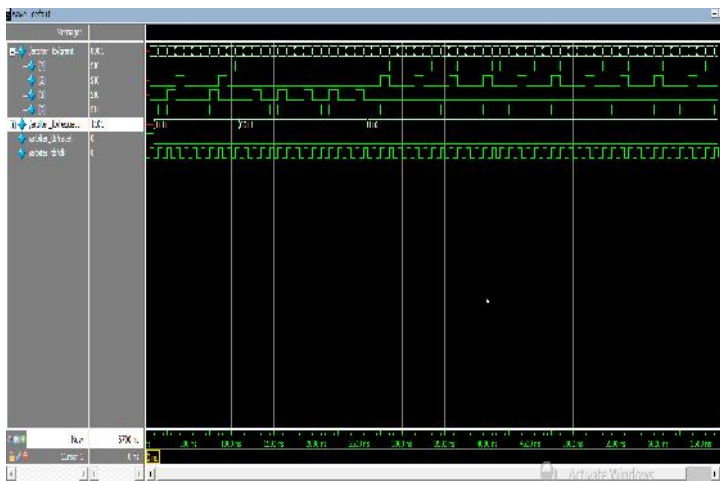


Figure 3: simulation result of the arbiter

A CPU (central processing unit) or DMA (direct memory access) can be used as the master of the AMBA AHB. We designed a DMA to act as master. Figure below shows the simulation result of the master.

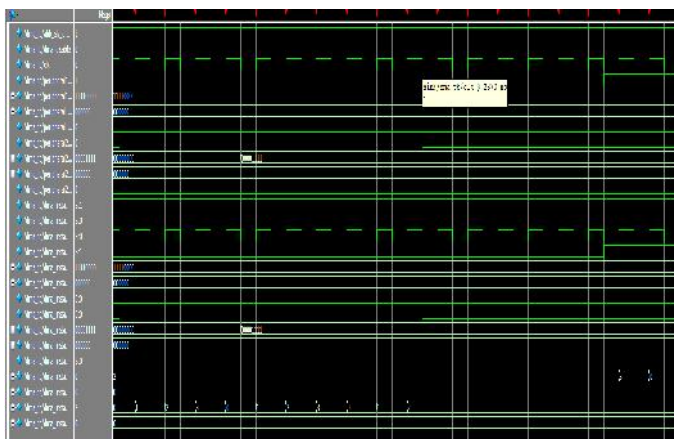


Figure 3: simulation result of the master

In the figure the above red triangle shows the message of assertion failure.

IV. VERIFICATION OF AHB ARBITER AND MASTER

Verification of the master and arbiter is done by writing assertions for the different PSL properties of the master and arbiter and then verified it using ModelSim tool. PSL assertions can be written in to the verilog code in two ways. It can be embedded in to the directly or it can be supplied through an external file. We embedded the PSL code directly in to the verilog file. Some of the PSL properties are given below in the table that are verified by writing assertions for it.

S. No	Property Description	Status
1	Master1 sends a request signal to the arbiter.	PASS
2	Master2 sends a request signal to the arbiter.	PASS
3	Master3 sends a request signal to the arbiter.	PASS
4	Arbiter gives a grant signal to the master1.	PASS
5	Arbiter gives a grant signal to the master2.	PASS
6	Arbiter gives a grant signal to the master2.	PASS
7	Arbiter is in idle state.	FAIL
8	Master1 first sends a request signal to the arbiter, but arbiter gives the grant signal to the master2.	FAIL
9	Master2 first sends a request signal to the arbiter, but arbiter gives the grant signal to the master3.	FAIL
10	Master3 first sends a request signal to the arbiter, but arbiter gives the grant signal to the master1.	FAIL

Table 1: PSL properties for arbiter

S. No	Property Description	Status
1	Master1 makes its bus request signal to high and drives the control and address signal to the bus.	PASS
2	Master2 makes its bus request signal to high and drives the control and address signal to the bus.	PASS
3	Master3 makes its bus request signal to high and drives the control and address signal to the bus.	PASS
4	Master1 does not response to the signal from slave1	FAIL
5	Master2 does not response to the signal from slave2	FAIL
6	Master3 does not response to the signal from slave3	FAIL

Table 2: PSL properties for master

V. CONCLUSION AND FUTURE WORK

In this paper assertion based functional verification is done by writing assertions for different PSL properties. Initially an AMBA AHB for 3 masters and 4 slaves is designed using verilog language and assertions for master and arbiter of the

AHB is written and verified in ModelSim. For the future work the assertion for the other part of the bus will also be written and verified and the total coverage report of the design will be calculated.

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